V100 Datasheet Brief

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Revision History

Date	Revision	Description
2016-07-22	1.0	First release

Introduction

Overview

V100 is a versatile high-performance, low-power and highly-integration SOC (system-on-a chip) tailored for 3D movie watching applications. It integrates MIPIS32 processor, together with the compact integrated video engine, display subsystem and audio engine deliever inmmersive 3D film experiences.
V100 supports up to 1080p video decoder. DDR2/DDR1 DRAM, SPI NOR, NAND Flash Controller with max 40-bit ECC and integrated RGB and LVDS LCD interface. Rich interfaces including USB 2.0, SDIO and other serial interfaces promote the system extension ablilities. V100 also integrated several regulators for power management which makes it the optimum choice for all-in-one entry level 3D movie display solutions with reasonable price.

CPU (Central Processing Unit)

- High Speed MIPS32 processor
- Support DSP ASE instruction extension
- 8-stage pipeline
- Programmable Memory Management Unit
- 16KB I-Cache and 16KB D-cache

CHIPID

- Programmable for customer

Video Decoder

- Support H.264 baseline/main/high profile decoding, up to 1080p resolution
- Support MPEG-4 SP/ASP decoding, up to 1080p resolution
- Support VC-1 simple/main profile decoding, up to 720p resolution
- Support MPEG1/2 decoding, up to 1080p resolution
- Support JPEG Baseline up to 8176*4080
- Support Rotation 90° & 270° fucntion
- Support Scale down function

Display Subsystem

• Dispay Engine

- Four moveable layers
- graphic layers, 1 YUV/RGB scaler video layer)
- Scaler input layer size up to 1920*1080
- Alpha blending and color space converting
- Dither function for 16 bit/18 bit interface LCD
- Gamma correction

- Support rotation and scale
- Video brightness, contrast and saturation adjustable

- **LCD/LVDS**

- Support active (TFT) LCD panels with digital RGB/CPU input interface
- Support single channel LVDS interface LCD
- LCD controller with 24-bit RGB color resolution support
- Resolutions up to 1280*800 or 800*1280
- Programmable timing control for various panels

Memory

- Support boot from
  - SPI NORFlash
  - NAND Flash

- **DDR**

- 16-bit DDR2/DDR1 DRAM controller, up to 64MByte
- 2.5V (SSTL_2 compatible) I/O for standard DDR1 device.
- 1.8V SSTL I/O for Standard DDR2

- **NAND Flash**

- 8-bit NAND Flash controller with 40-bit ECC
- SLC, MLC NAND Flash supported
- Monitor the NAND flash Ready/Busy signal by HW support

- **SD/MMC/SDIO**

- Support
  - SD/HCSD/SDXC
  - MiniSD
  - MicroSD
  - MS
  - MMC/RSMMC/MMCPLUS card
- Support 1 bit, 4bit, bus mode
- Support SDIO function
- Clock max rate up to 52MHz
- Read /Write CRC Status Hardware auto checked
- Support Auto multi Block read/write mode
- Hardware timeout/delay function
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing
- Build-in pull up resistance for CMD/DAT lines

Audio Engine

- Support MPEG 1/2/2.5 L1/L2/L3 decoding, 8~ 448K bps, CBR&VBR
- Support WMA decoding, up to 384Kbps, CBR&VBR
- Support AAC/OGG/APE decoding
- Support several formats Audio encoding
- Support I2S TX master mode, with sample rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96kHz
- Built-in stereo 20-bit DAC, SNR>98dB, SNR (A-Weighting)>99dB, THD+N<-86dB
- Built-in DAC supports sample rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48kHz
- Built-in ADC supports sample rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1/48kHz
- The ADC SNR>85dB, SNR (A-Weighting)>87dB, THD+N<-80dB

- Built-in stereo 20mW PA (Power Amplifier) for headphone.
- The anti-pop circuit for PA noise suppression

Highly-Integrated System peripherals

USB 2.0

- USB 2.0 device and host controllers
- Complies with the USB2.0 Specification Revision 1.0a.
- UTMI+ level2 Transceiver Macrocell Interface.
- Supports point-to-point communication with one full-speed or high-speed device in Host mode (no HUB support).
- Supports full-speed or high-speed in peripheral mode.
- Supports bulk Isochronous and Interrupt transfer.

SPI

- One SPI support master mode and slave mode. The speed of master mode is up to 80Mbps, and the sleep of slave up to 20Mbps.
- Support dual I/O write and read mode while use as master.
- Support single data rate mode and double data rate (DDR mode) while use as master.
- Support two wire mode, only use SCLK and MOSI signal.
- Support IRQ and DMA mode to transmit data.

TWI

- One TWI supports master and slave modes
- Support standard mode (100kbps) and fast-speed mode (400kpbs)
- Hi-speed mode and 10-bit address mode not support
- Internal Pull-Up Resistor (2.7kOhm) optional

UART

- One UART supports 5-8 Data Bits and LSB first in Transmit and Receive
- 1-2 Stop Bits
- Even, Odd, or No Parity
- Capable of speeds up to 1.5Mbps connecting with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data

IR Receiver

- Support de-bounce function
- Support RC5\RC6\9012\NEC(8bit) protocol, compatible 36kHz, 38kHz and 40kHz carriers

PWM

- 4 independent PWM signals from Hz to MHz
- PWM with 64-level duty adjustment
- PWM with high level or low level active
- Build-in pull-up or pull-down resistance in some functional pads

Power and others

- Integrated several LDOs for internal circuit
- Operating voltage: I/O 3.3V, Core 1.2V
- Low Power Consumption, less then 0.16mW/MHz of the CPU
- Dynamic system clock adjustment
- Support 6-channel 7-bit ADCs for system monitor and key matrix control

Package

- LQFP128

Application Diagram

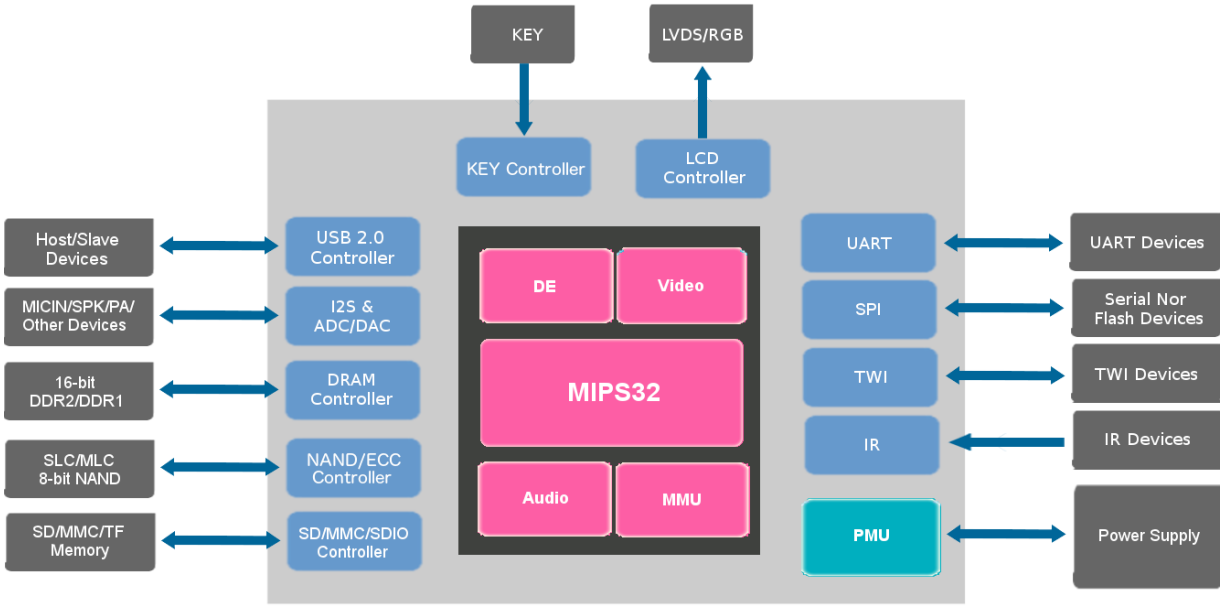

Figure V100 Application Diagram

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